LD7032

128 x 40 Mono OLED Column / Row
Driver with Controller

This document is a general product description and is subject to change without notice. LDT Inc. does NOT assume any responsibility use of circuits described.

1. REVISION HISTORY

Ver	CONTENS	DATE
1.0	- First version	Jun. 2008
2.0	- an addition : page7. or floating - deleted "When IXS=H, CSB must be Low" in page7 - AC Table : VDD = 1.65 ~ 3.5V (page24,26,27)	Dec. 2008

PART 1 CONTENTS

2. FEATURES

Power Supply

VDD : 1.65 ~ 3.5V
VCC_C : 8.0 ~ 16.0V for Column
VCC_R : 8.0 ~ 16.0V for Row

Display Area

Max 128 x 40 Line

Graphics RAM

Dot matrix : 128 x 1 Bit x 40 = 5,120 Bit

Column Driver

Max 128 Outputs
Mono
Maximum Output Current = 255 uA (1 uA Step)
Next Pin to Pin Current Deviation ± 2.0 (Iout = 50uA)
Current Deviation at 1Chip Max-Min ± 4.0 % (Iout = 50uA)
Average Current Deviation against absolute level ± 6.0% (Iout = 50uA)
5 Times Peak boot Current Driving

Row Driver

Max 40 Outputs
Variable duty ratio (1 to 40)
ON resistance typical 25ohm

CPU Interface

8080 or 6800 series parallel interface
Serial Peripheral Interface
I2C Serial Interface

Screen Saver

Screen Saver Function.

Oscillator

On-chip RC oscillator

Frame Rate

Variable Frame Rate (60,75,90,105,120,135)Hz

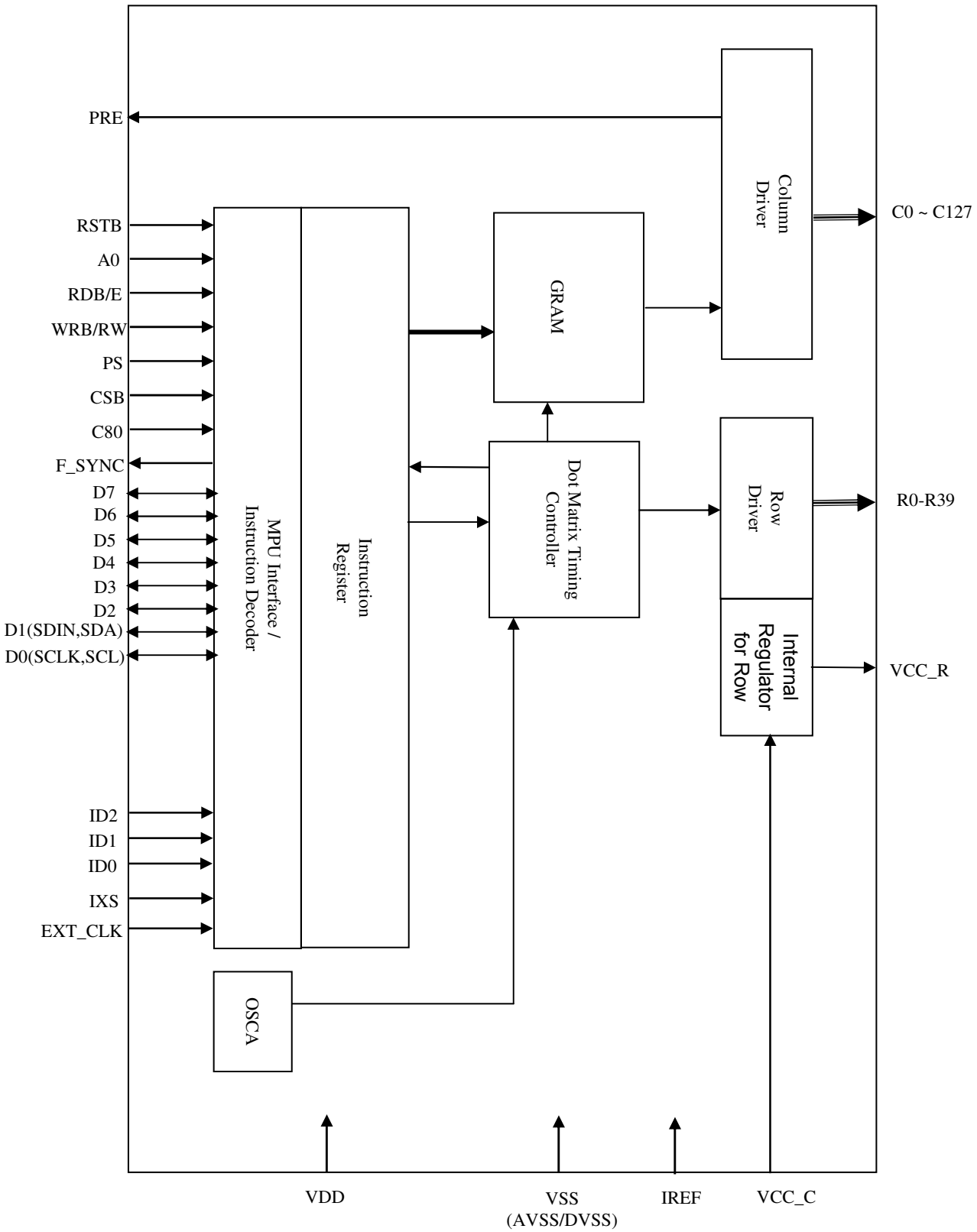
Crosstalk

Crosstalk enhancement function

Internal regulator for row driver

Selectable Voltage Function. (0.8*VCC_C or 0.7*VCC_C)

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

4. 1. Power Supply Pins

Signal	TYPE	Function
VCC_C	Power	OELD Dot Matrix Power Supply for Column Driver
VCC_R		OELD Dot Matrix Power Supply for Row Driver If Internal Regulator for Row Scan is active, this pin is the power output pin of internal row power regulator. A 4.7uF capacitor is recommended to connect between VCC_R and VSS. If internal row power regulator is disabled, it must be connected to the external high voltage source or VCC_C.
VDD		Analog and digital voltage supply.
VSS (AVSS/AVSS)		Ground pin.

4.2. System Interface Control Pins

Signal	TYPE	Function
C80	I	H: 68CPU L: 80CPU
PS	I	H: Parallel L: Serial
IXS	I	H : I2C is selected, L : I2C is not selected

*. Interface Mode Table

Interface Mode	PS	IXS
Parallel	1	X
Serial SPI	0	0
Serial I2C	0	1

4.3. MPU Interface Pins

Signal	TYPE	Function
CSB	I	Chip Select (Active Low)
RDB/E	I	Read (Active Low, 80 Interface) Enable (68 Interface)
WRB/RW	I	Write (Active Low, 80 Interface) H:Read L:Write (68 Interface)
RSTB	I	Reset (Active Low)
A0	I	Address (L: command, H: Parameter)
D7~D0	I/O	These are 8-bit bi-directional data bus to be connected to t he microprocessor's data bus. When I2C interface mode is selected, D1 will be the I2C d ata input (SDA) and D0 will be the I2C bus clock input (S CL), and D2 ~ D7 should be tied VDD or VSS. When serial interface mode is selected, D1 will be the seria l data input (SDIN), D0 will be the serial clock input (SCL K), and D2 ~ D7 should be tied VDD or VSS or floating.
ID2~ID0	I	These pins configure I^2C interface address. Using these pins, I^2C Address can be selected.
IREF	O	This pin is the dot output current reference pin. I_{DOT} is derived from Iref. A resister should be connected between this pin and VSS . (Current Setting. Typ Resistance = 39 kΩ) (Current adjustable range ±30%)
PRE	O	Pre-Charge Voltage
F_SYNC	O	Frame Sync Signal
EXT_CLK	I	Test Pin. This pin should be tied VDD or VSS in normal operation.

4.4. OLED Driver Pins

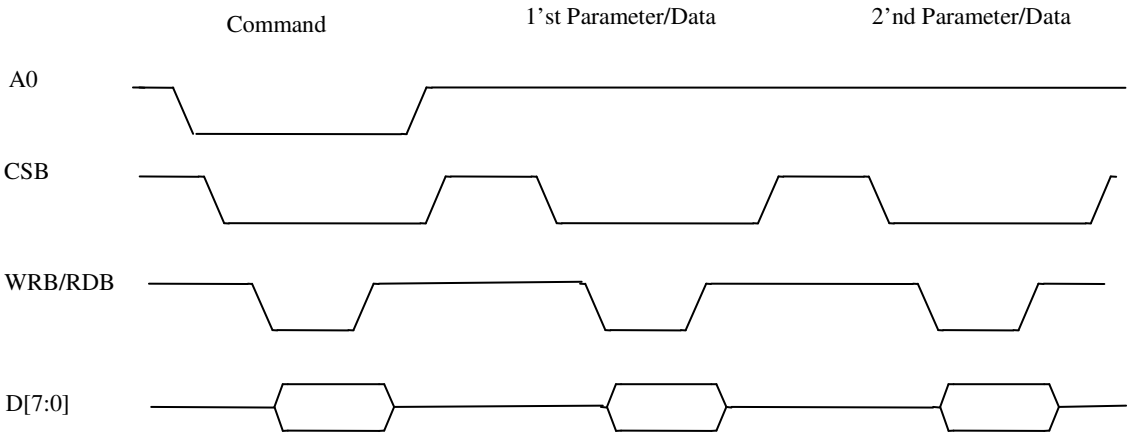
Signal	TYPE	Function
R0 to R39	O	OELD Dot Matrix Row Output
C0 to C127	O	OELD Dot Matrix Column Output

5. FUNCTIONAL DESCRIPTION

5.1 MPU Interface

5.1.1. 80 Series Interface

Function	CSB	WRB	RDB	A0	D[7:0]
Write Command	L	↑	H	L	Command
Write Parameter or Data	L	↑	H	H	Parameter or Data
Read Parameter or Data	L	H	↑	H	Parameter or Data



※NOTE :

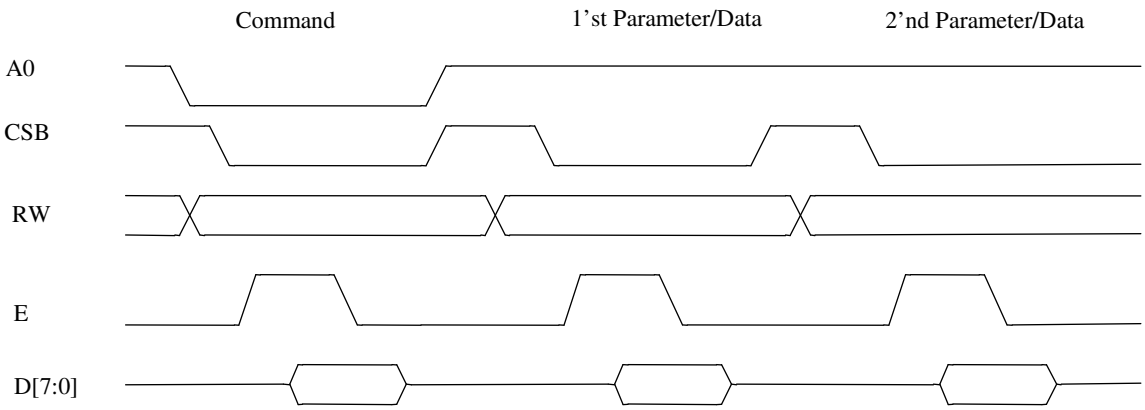
↑ stands for rising edge of signal.

L stands for low in signal.

H stands for high in signal.

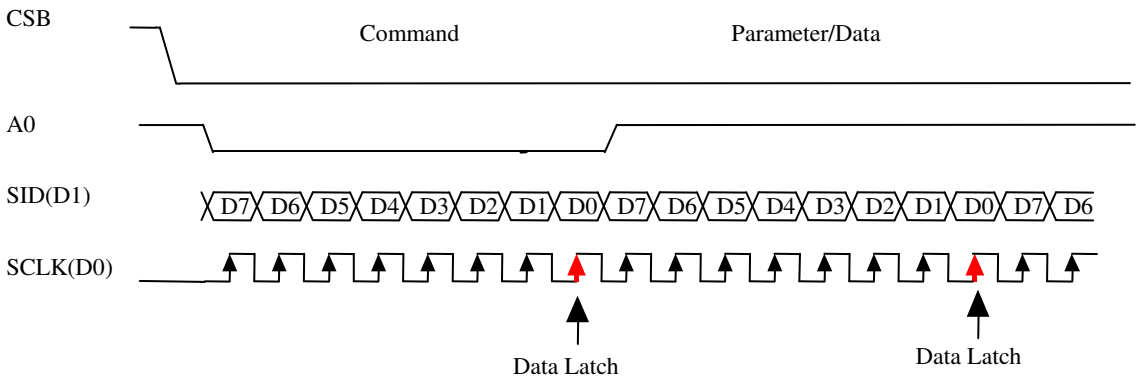
5.1.2. 68Series Interface

Function	CSB	RW	E	A0	D[7:0]
Write Command	L	L	↓	L	Command
Write Parameter/Data	L	L	↓	H	Parameter or Data
Read Parameter/Data	L	H	↓	H	Parameter or Data



5.1.3. Serial Interface

Function	CSB	CLOCK	A0	DATA
Write Command	L	D[0]	L	D[1]
Write Parameter/Data	L	D[0]	H	D[1]



※ Notice
- All command inputs have a priority over previous commands.
- To select Parallel/Serial Interface use PS Input. (H: Parallel L: Serial)
- Serial clock (SCLK) works in the unit of 8 clocks.

5.1.4. I2C Interface

The bidirectional I2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I2C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse.

On the I2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 2).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly,
the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

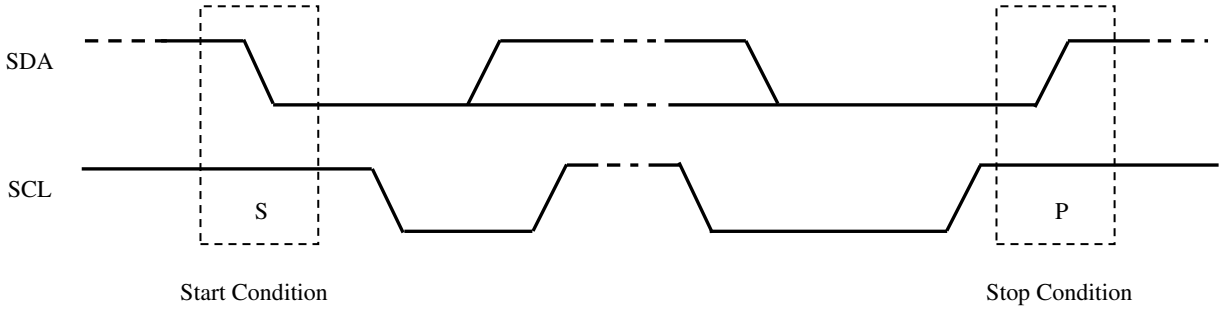


Figure 1. Definition of Start and Stop Conditions

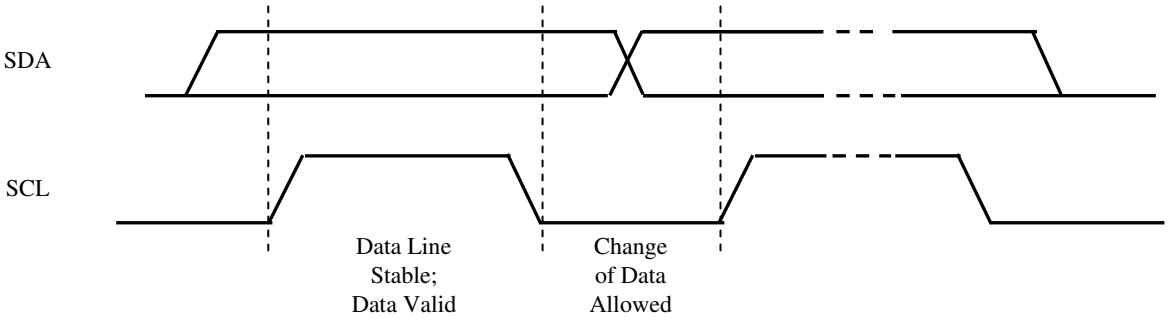


Figure 2. Bit Transfer

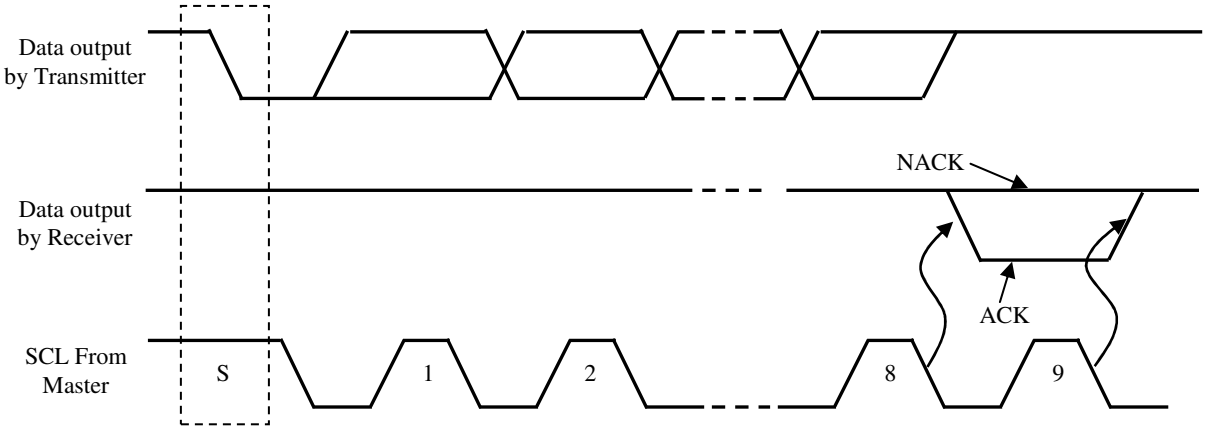


Figure 3. Acknowledgement on I2C Bus

- I2C Device ID Address

Following a START condition, the bus master must output the address of the slave it is accessing. The address is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

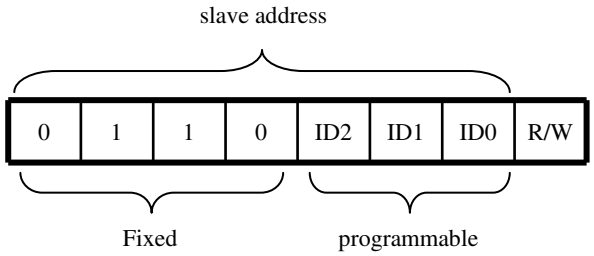


Figure 4. Device ID Address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

MSB bit is first transfered.

- I2C Bus Transactions

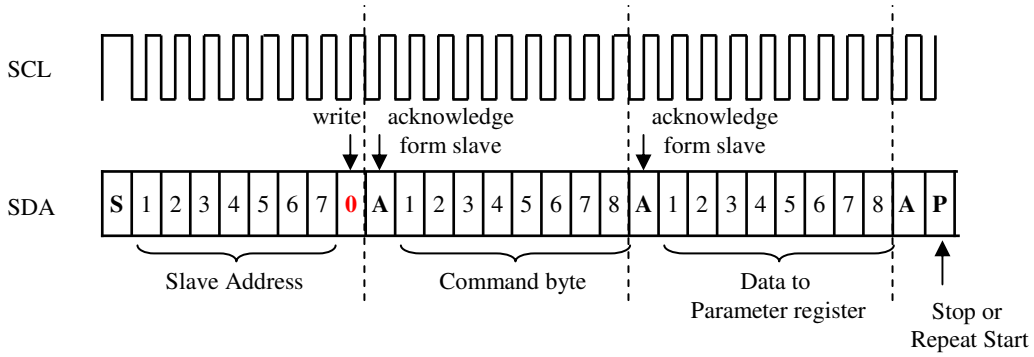


Figure 5. Write Single Parameter Command

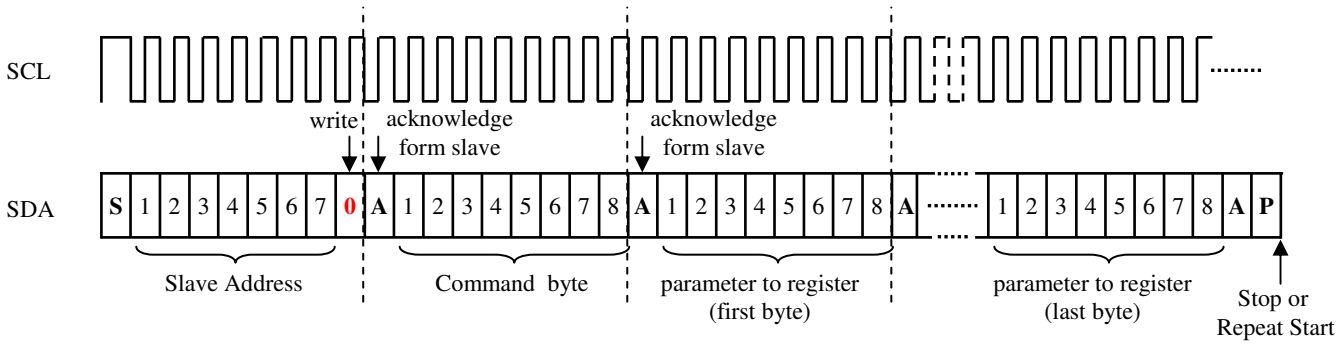


Figure 6. Write Multi Parameter Command

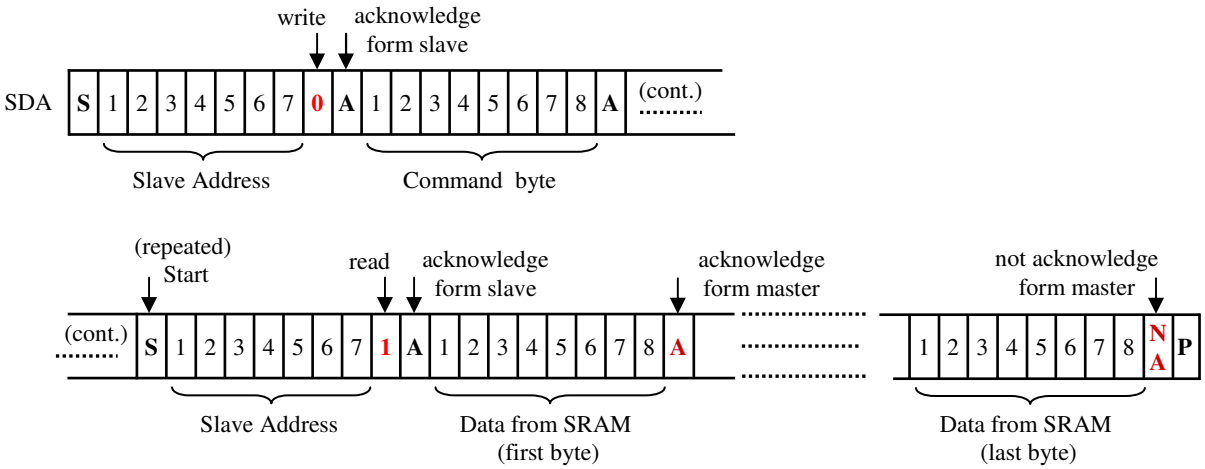
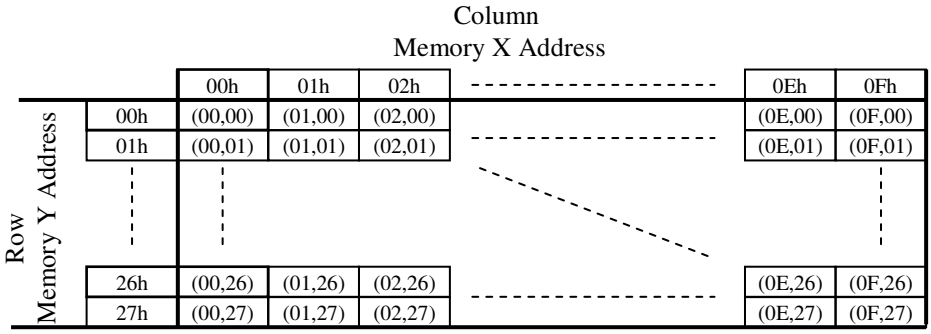


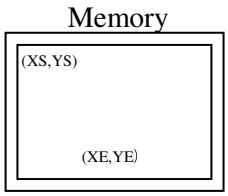
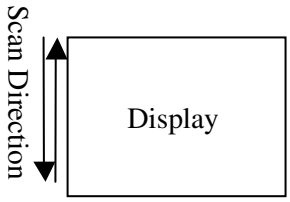
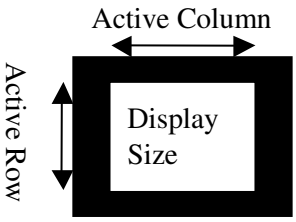
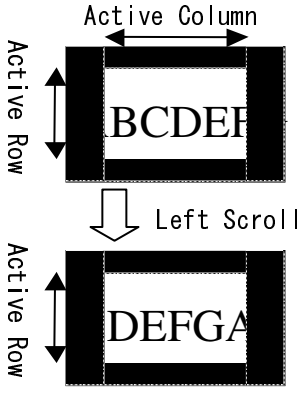
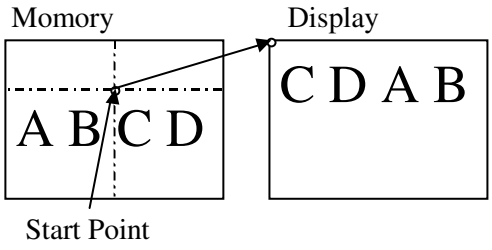
Figure 7. Read From SRAM

5.2 Dot Memory Map

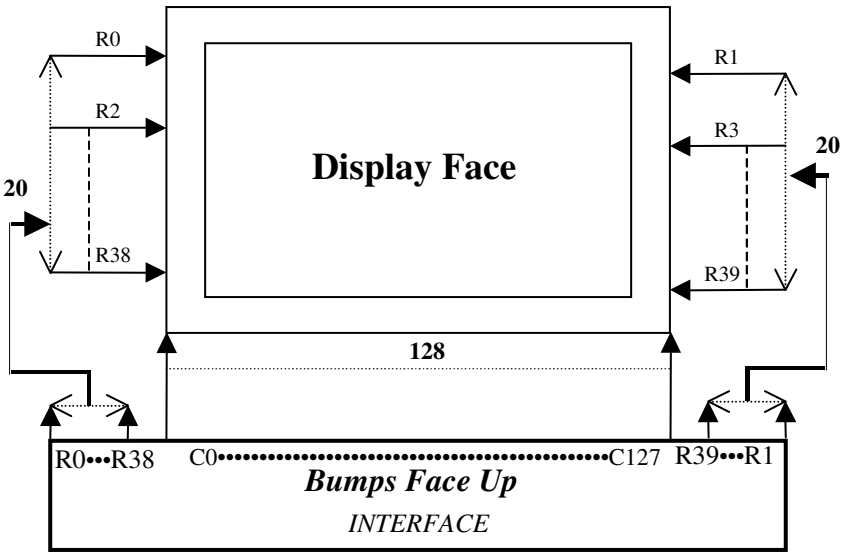


Memory Size = 16 x 8Bit x 40 = 5,120 Bit

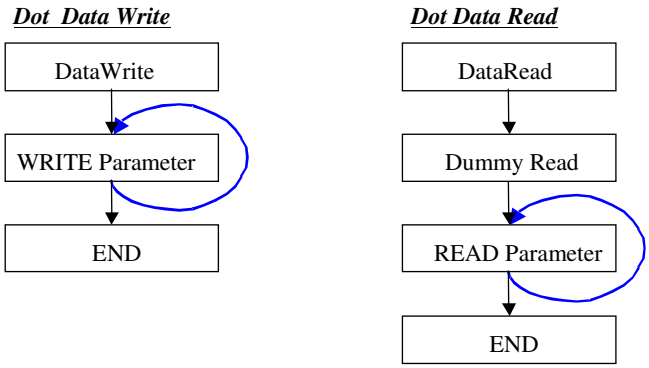
5.3. Correspondence Memory and Display

Memory Data Write	- "Data Writing Box" command indicate memory writing area. - "Writing direction" command indicate writing direction (auto address increment or decrement)	
Display Direction	- "DispDirection" command indicate Row scan direction. - Row R0⇔Rmax	
Display Size	- "DispSize" command indicate active outputs. - The column outputs out of active area always pre-charge level. - The row outputs out of active area always VCC_R excluding display off. - Scan is repeated within active area. - Rows out of active row are VCC_R. - "DispSize" command don't use during panel display.	
Scroll Area	- In scroll mode, display all memory area regardless display size.	
Memory Reading Start Address	- "DispStart" command fix the relation of memory and display coordinates.	

5.4. Output Arrange

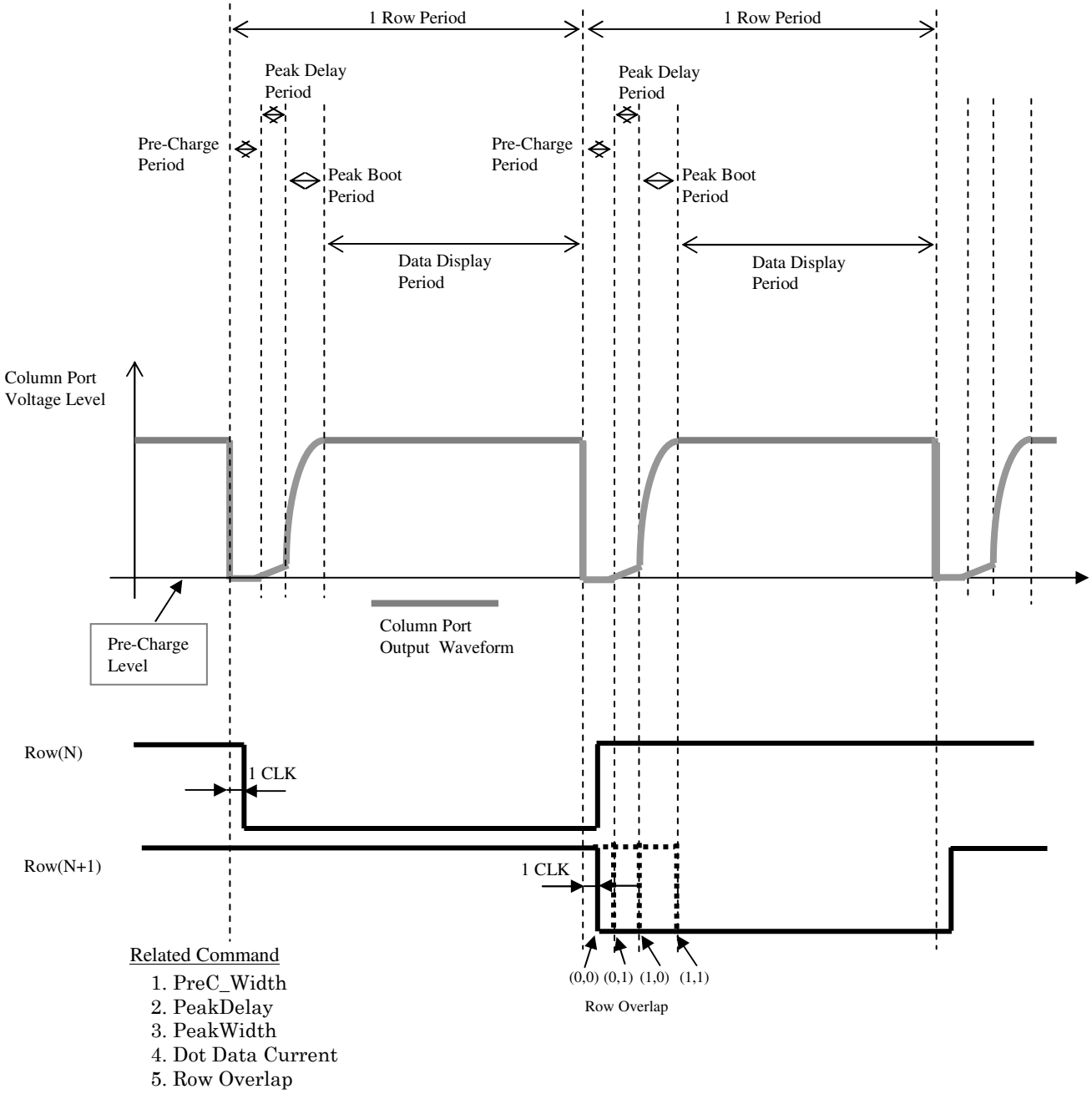


5.5. Data Write / Read Sequence



 Serial Interface is impossible to Data Read

5.6. Dot Matrix Output Wave Form



Related Command

1. PreC_Width
2. PeakDelay
3. PeakWidth
4. Dot Data Current
5. Row Overlap

5.7. Pre-charge

When Pre-Charge, each column output is connected the pre-charge pin in the IC. Therefore all dot matrix column outputs have the switch between driver and pre-charge pin

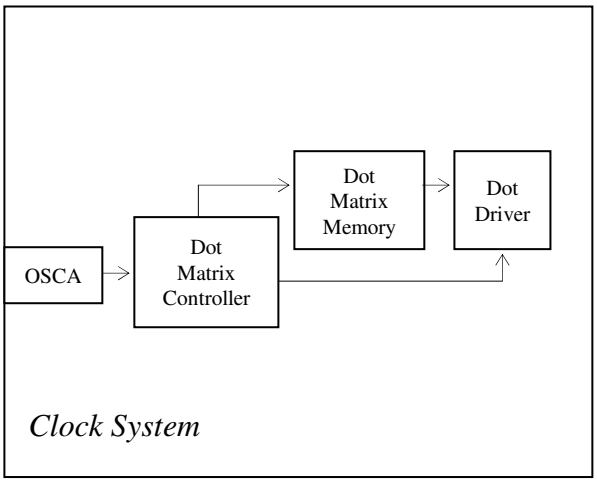
5. 8. Power Save

	Function	Display ON/OFF	Stand-by	Soft Reset
Dot Matrix	Command	DISPON/OFF	STBON/OFF	SOFTRES
	Function	• Display ON/Off	• Display-OFF • OSCA Start/Stop	• Register Clear • Display-OFF • Stand-by-ON

5. 9. Reset

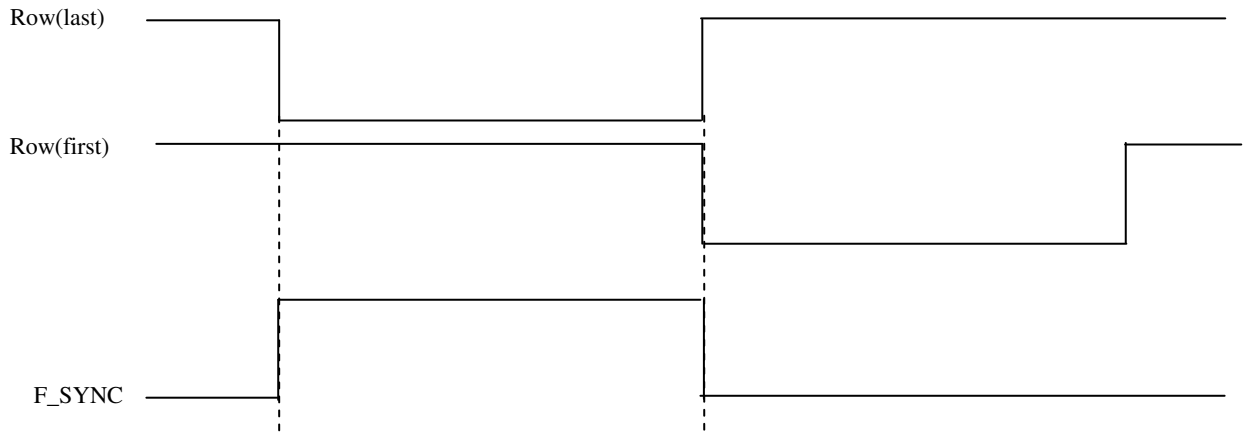
When RSTB Input becomes 'L', All Register is set Default.
When SOFTRES command is inputted, All Register is set Default

5. 10. OSC



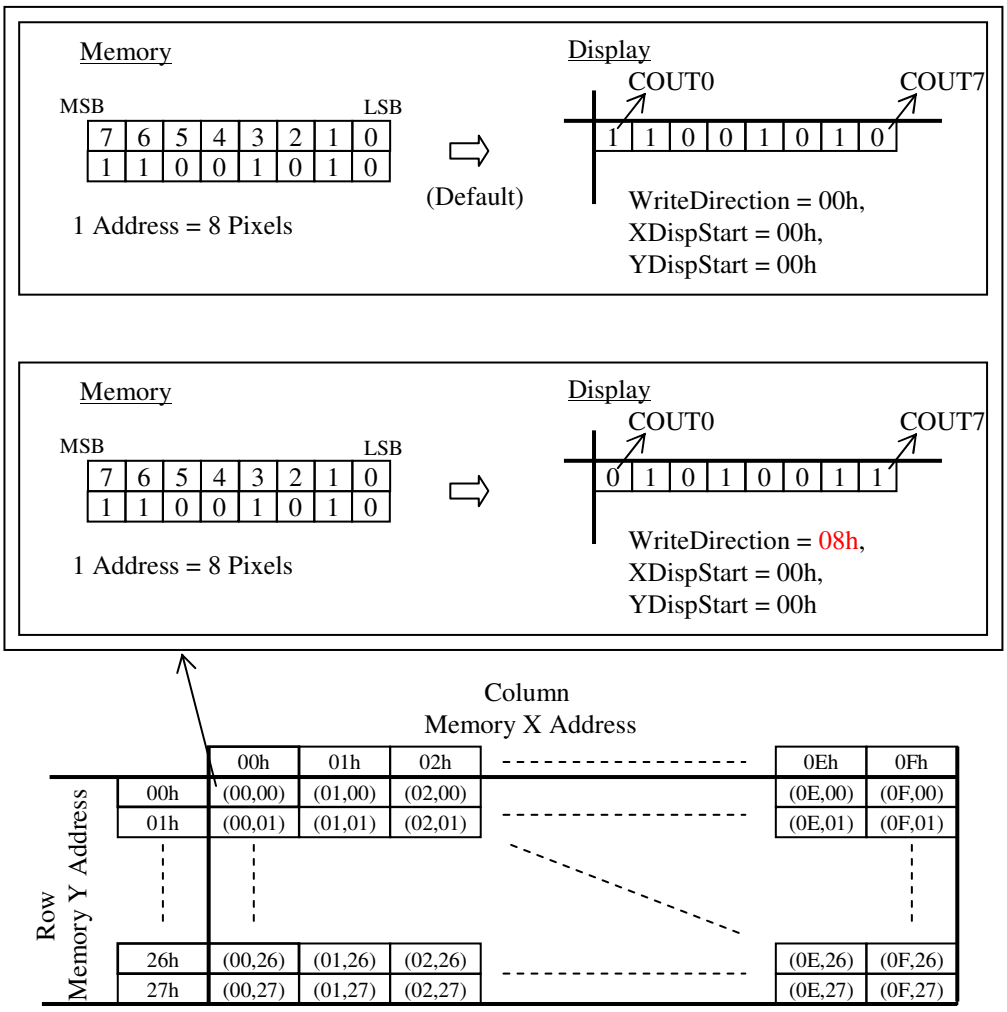
- In stand-by mode, oscillator is stopped.
- Frame frequency is adjusted by "DFRAME" command

5. 11. Frame Sync Signal (F_SYNC)



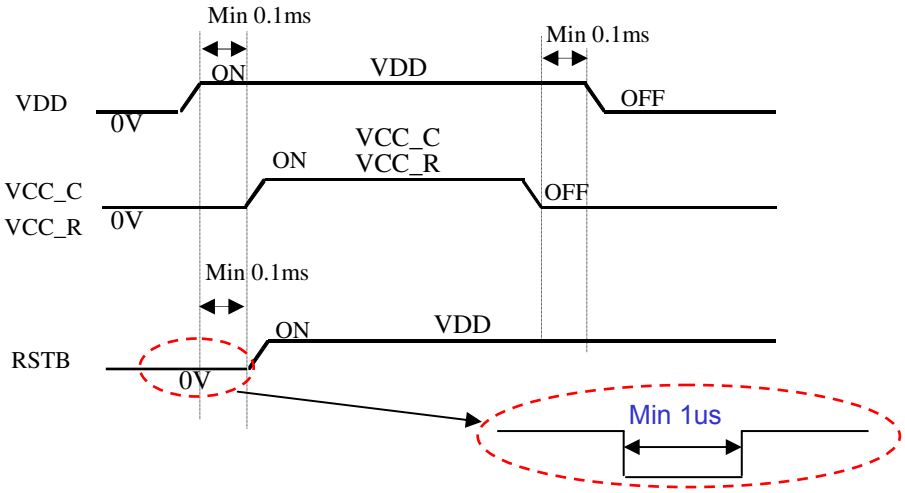
5. 12. Interface Mode (Data Write Only)

Dot matrix display data write mode



6. Referential Set-up Flow

6.1 Power ON-OFF



7. ELECTRICAL CHARACTERISTICS

7.1 MAXIMUM RATINGS

(Ta = -40 ~ 85℃)

content	Parameter	Value	Unit
VDD	Supply Voltage	**−0.3～+3.63**	
VCC_C		**-0.3～+18.0**	
VCC_R		**-0.3～+18.0**	V
V_{IN}	Input Voltage Range	**−0.3～VDD+0.3**	
V_{OUT}	Output Voltage Range	**−0.3～VDD+0.3**	
T_{OPR}	Operating Temperature Range	**−40～+85**	℃
T_{STG}	Storage temperature Range	**−50～+125**	℃

7.2. DC CHARACTERISTICS

(VDD= 2.8V, VCC_C=VCC_R=15V, Ta = 25℃)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	UNIT
VCC_C	Operating Voltage for Column	-	VCC_C	8	-	16	V
VCC_R	Operating Voltage for Row	-	VCC_R	8	-	16	
VDD	Logic Power 1	-	VDD	1.65	1.8 2.8	3.5	
V_{IH}	High Logic Input Level	-	Logical Input	0.8*VDD	—	VDD	
V_{IL}	Low Logic Input Level	-	Logical Input	0	—	0.2*VDD	
V_{OH}	High Logic Output Level	Iout＝-100uA	Logical Output	0.9*VDD	—	VDD	
V_{OL}	Low Logic Output Level	Iout＝100uA	Logical Output	0	—	0.1*VDD	
IIL	Input Leakage Current			－1.0		+1.0	uA
FOSC1	Oscillator Frequency For Dot Matrix	VDD = 2.8V VDD = 1.8V		0.9 0.82	1.0 0.91	1.1 1	MHz
IRVCC	VCC_R Power Regulator Output Voltage	VCC_R = 0.8*VCC_C I_{VCC_R}=5mA	VCC_R	0.75* VCC_C	0.8* VCC _C	0.85* VCC_C	V
Cptp1	Output Current Pin to Pin Even ness *1)	Iout = 50uA	C0-127	－2.0	—	+ 2.0	%
Calp1	Output Current Evenness *2)	Iout = 50uA	C0-127	－4.0	—	+ 4.0	%
Cchip1	Output Current Absolute Correctness *3)	Iout = 50uA	C0-127	－6.0	—	+ 6.0	%
Cptp3	Peak boot Pin to Pin Evenness *1)	Ioutpeak = 250uA	C0-127	－2.0	—	+ 2.0	%
Calp3	Peak boot Evenness *2)	Ioutpeak = 250uA	C0-127	－4.0	—	+ 4.0	%
Cchip3	Peak boot Absolute Correctness *3)	Ioutpeak = 250uA	C0-127	－6.0	—	+ 6.0	%
Rrg	ROW - Vss ON Resistance	IOL=35ｍA	R0-R39	-	25	40	Ω
Rr	ROW - VCC_R ON Resistance	IOL=1ｍA	R0-R39	-	1	3	kΩ

NOTICE:

*1) (Ik － I k+1)/ Iavg ： (k = 0 to 127), Iavg = Σ (Ik) / 128 ： (k = 0 to 127)

*2) (Imax－Iavg) / Iavg , (Imin－Iavg) / Iavg , Iavg = Σ (Ik) / 128 ： (k = 0 to 127)

*3) (Iavg－Iref(SPEC)) / Iref(SPEC)

(VDD= 2.8V, VCC_C=VCC_R=15V, Ta = 25℃)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	UNIT
Rp	Pre-Charge SW ON Resistance	Each Pin ILOAD=3mA	C0-127	—	600	900	Ω
		Column All Pin Short	C0-127	—	—	7	Ω
IVDD1	Stand-by Current		VDD	—	-	5	uA
IVCC_C1			VCC_C		-	5	uA
IVCC_R1			VCC_R		-	5	uA
IVDD2	Normal Operation	*4)	VDD		-	1	mA
IVCC_C2		*4)	VCC_C		-	2	mA
IVCC_R2		*4)	VCC_R		-	1	mA

NOTICE:

*4) Iout =10μA, All Data on, Frame Frequency 120Hz, VCC_C=VCC_R=15V, VDD=2.8V, Output(DOT) all Open, Display Size full, Others Default

(VDD= 2.8V, VCC_C=VCC_R=15V, Ta = 25℃)

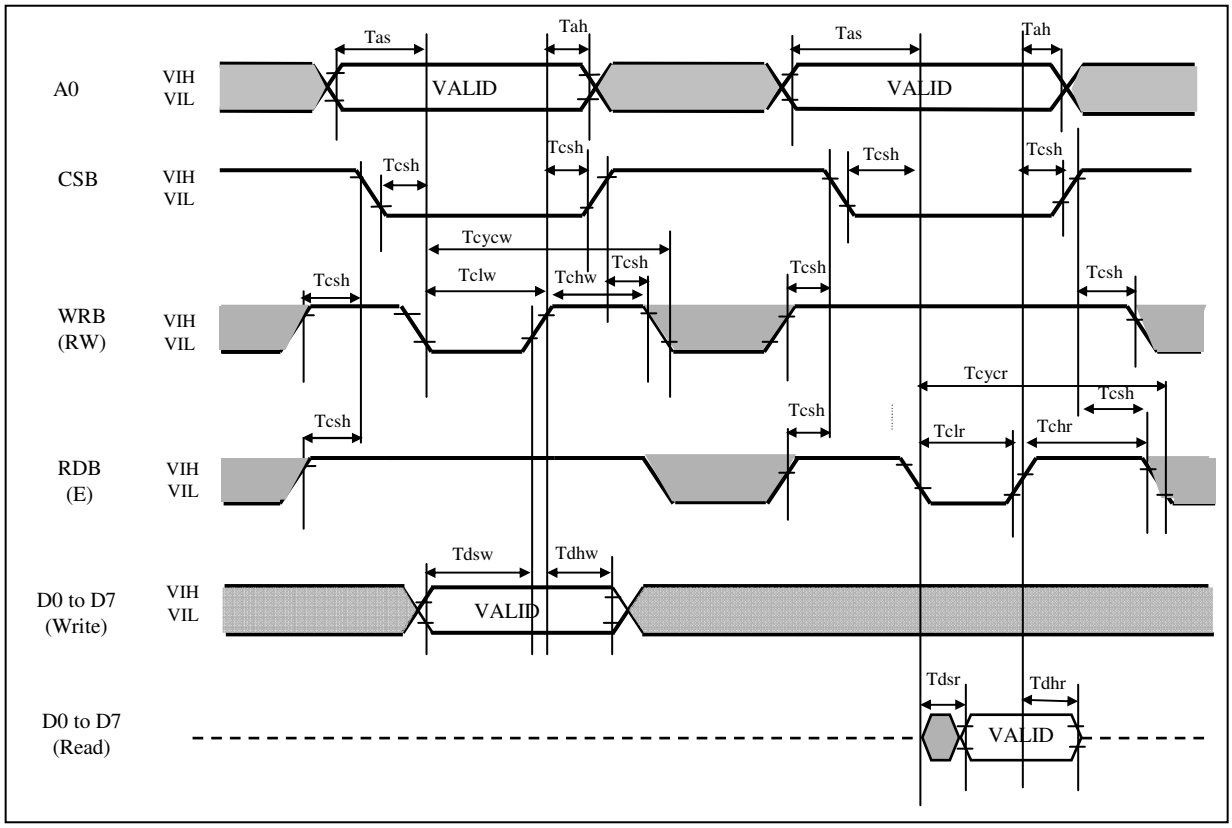
Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{OL}	Low Logic Output Level (open-drain) at 3mA sink current at **SDA, SCL (I²C)**	V_{DD} > 2V	0.0	—	0.4	V
		V_{DD} < 2V	0.0	—	0.2*V_{DD}	
I_{OL}	Low-Level output Current (I²C)	VOL = 0.4V	3	-	-	mA
		VOL = 0.6V	6	—	-	

7. 3. AC Characteristics

7. 3. 1.1 Parallel Interface1 (Write/Read Timing)

(VSS = 0V, VDD= 2.6V~3.5V, Ta = 25℃)

Parameter	Symbol	Condition		Specification MIN	Specification MAX	Units
Address setup time	Tas	A0		20		ns
Address hold time	Tah	A0		10		
System cycle time	Tcycw	WRB	Write	100		
	Tcycr	RDB	Read	500		
Write control low pulse width	Tclw	WRB		40		
Write control high pulse width	Tchw			40		
Read control low pulse time	Tclr	RDB		60		
Read control high pulse time	Tchr			80		
Write data setup time	Tdsw	D0 – D7		20		
Write data hold time	Tdhw			10		
Read data setup time (Data Output Access Time)	Tdsr				200	
Read data hold time (Data output disable time)	Tdhr			10		
CSB – WRB , RDB time	Tcsh	CSB		10		

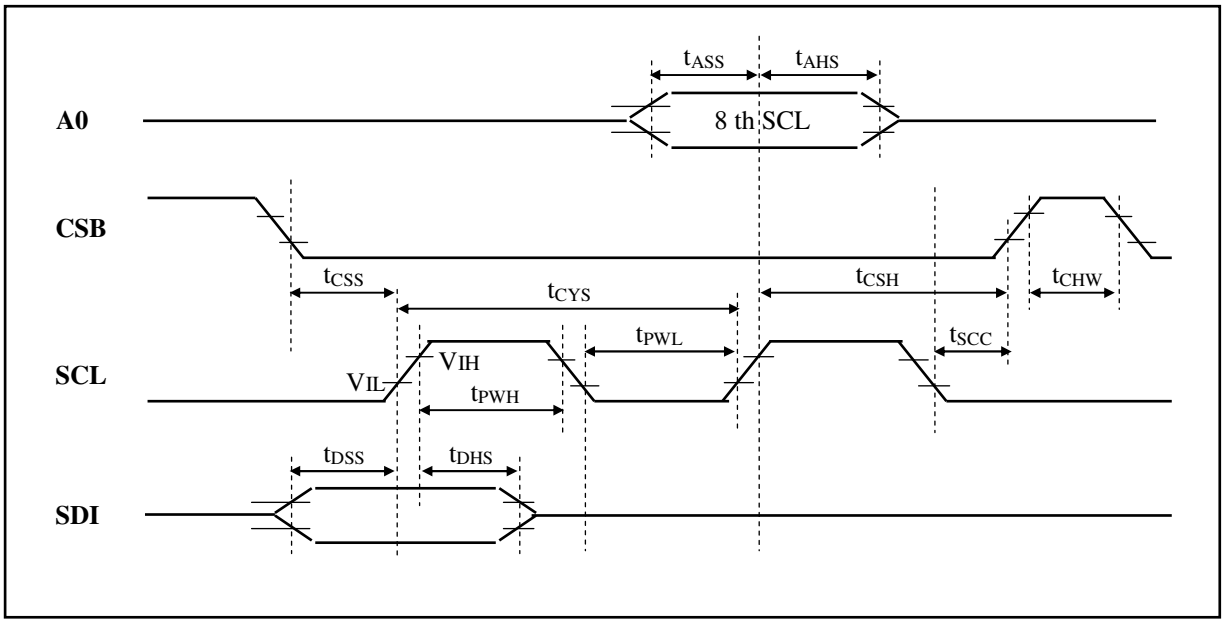


7. 3. 1.2 Parallel Interface2 (Write/Read Timing)

(VSS = 0V, VDD= 1.65V~3.5V, Ta = 25℃)

Parameter	Symbol	Condition		Specification		Units
				MIN	MAX	
Address setup time	Tas	A0		60		ns
Address hold time	Tah	A0		30		
System cycle time	Tcycw	WRB	Write	300		
	Tcycr	RDB	Read	500		
Write control low pulse width	Tclw	WRB		120		
Write control high pulse width	Tchw			120		
Read control low pulse time	Tclr	RDB		60		
Read control high pulse time	Tchr			80		
Write data setup time	Tdsw	D0 – D7		60		
Write data hold time	Tdhw			30		
Read data setup time (Data Output Access Time)	Tdsr				200	
Read data hold time (Data output disable time)	Tdhr			10		
CSB – WRB , RDB time	Tcsh	CSB		30		

7. 3. 2.1 Serial Interface1

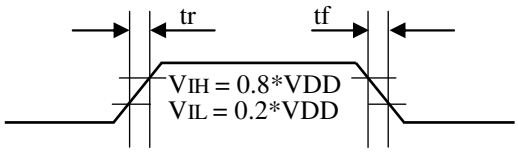


(VSS = 0V, VDD= 2.6V~3.5V, Ta = 25℃)

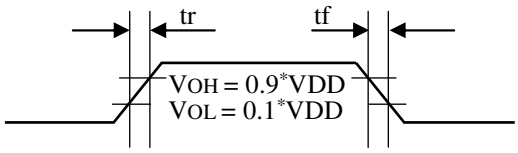
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CYS} t_{PWH} t_{PWL}	Serial clock cycle High pulse Width Low pulse width	-	SCL	66 20 20	- -	- -	ns
t_{ASS} t_{AHS}	A0 setup time A0 hold time		A0	15 25	- -	- -	ns
t_{DSS} t_{DHS}	Data setup time Data hold time		SDI	20 20	- -	- -	ns
t_{CSS} t_{CSH} t_{CSW}	Chip select setup time Chip select hold time Chip select high pulse width	-	CSB	20 50 50	- - -	- - -	ns
t_{SCC}	SCL to Chip select	-	SCL, CSB	15	-	-	ns

NOTE : The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



7. 3. 2.2 Serial Interface2

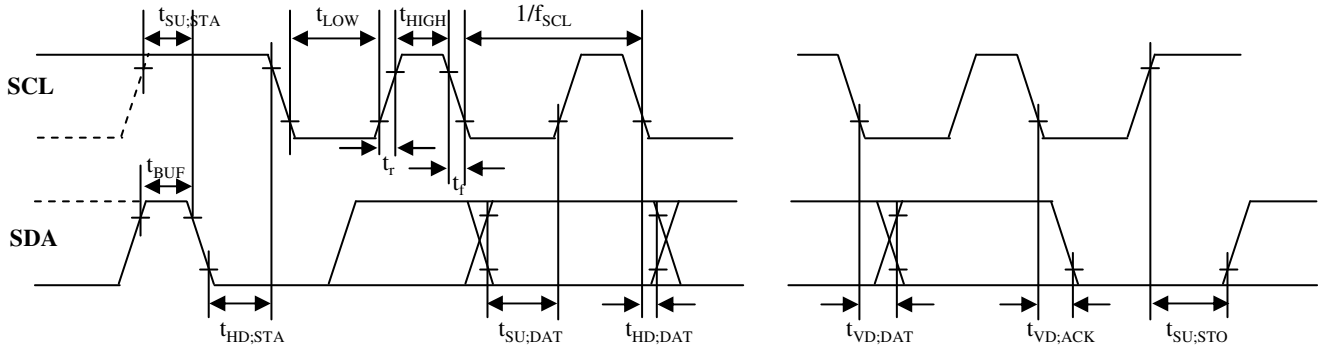
(VSS = 0V, VDD= 1.65V~3.5V, Ta = 25℃)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CYS} t_{PWH} t_{PWL}	Serial clock cycle High pulse Width Low pulse width	-	SCL	150 60 60	- -	- -	ns
t_{ASS} t_{AHS}	A0 setup time A0 hold time		A0	50 60	- -	- -	ns
t_{DSS} t_{DHS}	Data setup time Data hold time		SDI	60 60	- -	- -	ns
t_{CSS} t_{CSH} t_{CSW}	Chip select setup time Chip select hold time Chip select high pulse width	-	CSB	60 100 100	- - -	- - -	ns
t_{SCC}	SCL to Chip select	-	SCL, CSB	40	-	-	ns

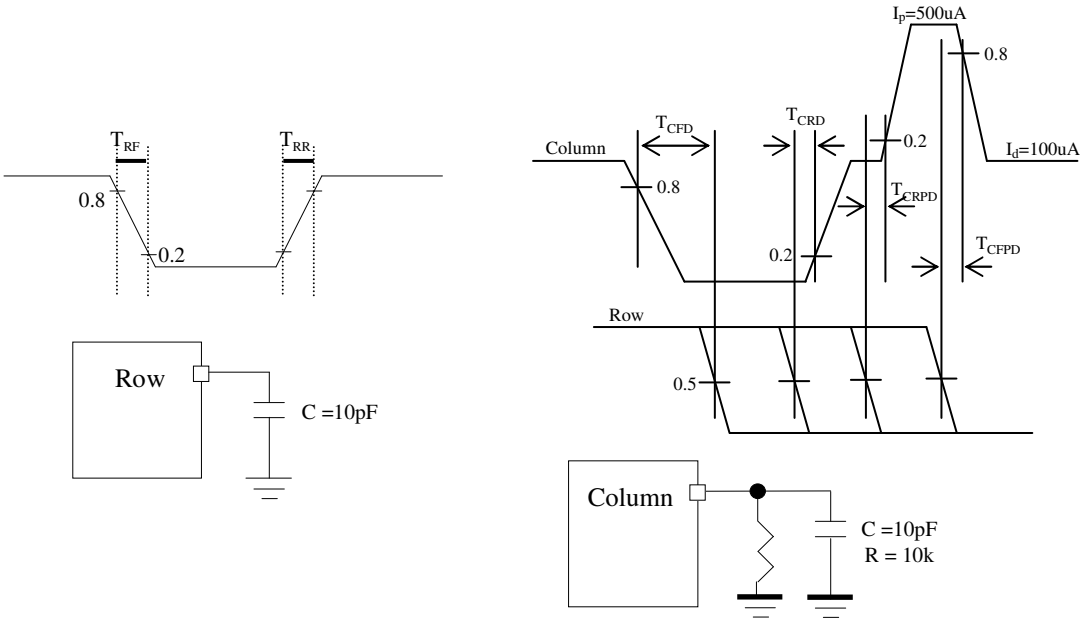
7. 3. 3 I2C Interface

(VSS = 0V, VDD= 1.65V~3.5V, Ta = 25℃)

Symbol	Parameter	Standard mode		Fast mode		Unit
		MIN	MAX	MIN	MAX	
f_{scl}	SCL clock frequency	0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition	4.7	-	1.3	-	us
$t_{HD;STA}$	hold time (repeated) START condition	4.0	-	0.6	-	us
$t_{SU;STA}$	set-up time form a repeated START condition	4.7	-	0.6	-	us
$t_{SU;STO}$	set-up time for STOP condition	4.0	-	0.6	-	us
$t_{SU;DAT}$	data set-up time	250	-	100	-	ns
$t_{HD;DTA}$	data hold time	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	0.3	3.45	0.1	0.9	us
$t_{VD;DAT}$	data valid time	300	-	50	-	ns
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	us
t_f	fall time of both SDA and SCL signals	-	300	-	300	ns
t_r	rise time of both SDA and SCL signals	-	1000	-	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns



7.3.4. Driver OUTPUT



Gray Scale	Normal Current	Peak Boot Current
0h	0uA	0uA
1h	IREF	IREF x 5 *1)

*1) 5 Times is guaranteed until 500 μ A

“RowOverlap” command changes Row falling timing`

(VSS = 0V, VDD= 2.6V~3.5V, VCC_C=VCC_R=15V, Ta = 25℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Row Falling Time	R0-R39	T_{RF}	-	-	10	ns
Row Rising Time	R0-R39	T_{RR}	-	-	100	ns
Column Falling Time until Row Falling	C0-C127 (to R)	T_{CFD}	800	-	1200	ns
Column Drive Start Delay Time	C0-C127 (to R)	T_{CRD}	0	-	200	ns
Column Peak Delay Time	C0-C127 (to R)	T_{CRPD}	0	-	200	ns
Column Peak Falling Delay Time	C0-C127 (to R)	T_{CFPD}	0	-	200	ns

7.3.5. Reset
Reset low pulse width must be long than 1 us.
Reset complete time is small than 1 us.

128 x 40 Mono OLED Column / Row Driver with Controller

PART 2 CONTENTS

INSTRUCTION DESCRIPTION

1. Display System Command

1.1 Software Reset

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
SOFTRES	W	L	**01h**	-	-	-	-	-	-	-	-	-	-	Software Reset	-

- Software reset command
- All registers are cleared default. *1)
- Dot matrix is OFF.
- OSCA is stopped

*1) Don't clear Graphics memory

1.2. Dot Matrix Display ON/OFF

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
DDISPON/OFF	W	L	**02h**	W	H	-	-	-	-	-	-	-	D0	D=0 Dot Matrix Display OFF D=1 Dot Matrix Display ON	00h

- When D0="0" :
  Turns the dot matrix Display OFF (Default).
  Display OFF means
  All Column Output become Pre-charge level.
  All Row Output become VSS.
  Stop Data transfer from memory to Dot Matrix Driver.

- When D0="1" :
  Turns the dot matrix Display ON.

1.3. Dot Matrix Display Stand-by ON/OFF

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
DSTBYON/OFF	W	L	**14h**	W	H	-	-	-	-	-	-	-	D0	D=0 : Stand-by OFF D=1 : Stand-by ON	01h

- When D0="0"
  OSCA Start. (Don't turn the dot matrix display on)

- When D0="1"
  Execute DDISPOFF command
  OSCA Stop. (Default).

*NOTE 1 : Don't clear Graphics memory and Register.
*NOTE 2 : After software and hardware Reset, stay "DSTBYON" Mode.
*NOTE 3 : Column Driver latched datas are reset.

1.4. Dot Matrix Frame Rate

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
DFRAME	W	L	**1Ah**	W	H	-	-	FO	M1	M0	F2	F1	F0	Frame Frequency 60-120Hz	02h

Dot Matrix frame rate control command.

Parameter Definition

F[2:0]	Frame Frequency *1)	**The Number of SCLK of one Row (Display Y Size = 32)**
0	60Hz	**520**
1	75Hz	**416**
2	90Hz(Default)	**346**
3	105Hz	**298**
4	120Hz	**260**
5,6,7	135Hz	**230**

◆ OSCA mode selection
M[1:0] = 00 Internal RC Oscillation mode
= 10 External Clock mode (Test Mode)

*1) FO = '0'
Frame frequency is difference value by [Display Y Size].
For Example : { F[2:0] = 010b, Display Y Size = 32 } => Frame Frequency is 90Hz. : Freq(SCLK) = 1.0MHz
{ F[2:0] = 010b, Display Y Size = 16 } => Frame Frequency is 180Hz. : Freq(SCLK) = 1.0MHz
{ F[2:0] = 010b, Display Y Size = 40 } => Frame Frequency is 72Hz. : Freq(SCLK) = 1.0MHz

Example 1) FO = '0'

F[2:0]	Frame Frequency (Spec.)	Display Y Size	Frame Frequency (Measured)	SCLK Freq. (MHz)	**F[2:0]**	Frame Frequency (Spec.)	Display Y Size	Frame Frequency (Measured)	SCLK Freq. (MHz)
0	60 Hz	16	120 Hz	1	**3**	105 Hz	16	210 Hz	1
		32	60 Hz	1			32	105 Hz	1
		36	53 Hz	1			36	93 Hz	1
		40	48 Hz	1			40	84 Hz	1
1	75 Hz	16	150 Hz	1	**4**	120 Hz	16	240 Hz	1
		32	75 Hz	1			32	120 Hz	1
		36	67 Hz	1			36	107 Hz	1
		40	60 Hz	1			40	96 Hz	1
2	90 Hz	16	180 Hz	1	**5,6,7**	135 Hz	16	270 Hz	1
		32	90 Hz	1			32	135 Hz	1
		36	80 Hz	1			36	120 Hz	1
		40	72 Hz	1			40	108 Hz	1

*1) FO = '1'
In this cases [Display Y Size = 16], [Display Y Size = 32]
frame frequency is same value.
For Example : { F[2:0] = 010b, Display Y Size = 32 } => Frame Frequency is 90Hz. : Freq(SCLK) = 1.0MHz
{ F[2:0] = 010b, Display Y Size = 16 } => Frame Frequency is 90Hz. : Freq(SCLK) = 0.5MHz

*** Note : " 0 < [Display Y Size] ≤ 16 " → [Freq(SCLK) = 0.5MHz]**

Example 2) FO = '1'

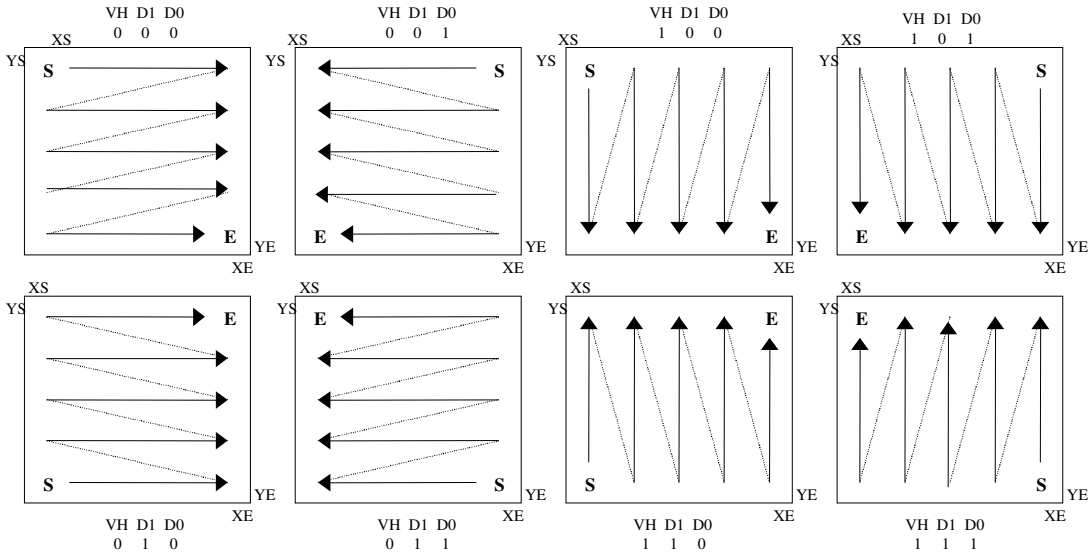
F[2:0]	Frame Frequency (Spec.)	Display Y Size	Frame Frequency (Measured)	SCLK Freq. (MHz)	**F[2:0]**	Frame Frequency (Spec.)	Display Y Size	Frame Frequency (Measured)	SCLK Freq. (MHz)
0	60 Hz	16	60 Hz	0.5	**3**	105 Hz	16	105 Hz	0.5
		32	60 Hz	1			32	105 Hz	1
		36	53 Hz	1			36	93 Hz	1
		40	48 Hz	1			40	84 Hz	1
1	75 Hz	16	75 Hz	0.5	**4**	120 Hz	16	120 Hz	0.5
		32	75 Hz	1			32	120 Hz	1
		36	67 Hz	1			36	107 Hz	1
		40	60 Hz	1			40	96 Hz	1
2	90 Hz	16	90 Hz	0.5	**5,6,7**	135 Hz	16	135 Hz	0.5
		32	90 Hz	1			32	135 Hz	1
		36	80 Hz	1			36	120 Hz	1
		40	72 Hz	1			40	108 Hz	1

1.5. Graphics Memory Writing Direction

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	
WriteDirection	W	L	**1Dh**	W	H	-	-	-	-	D3	VH	D1	D0	D1:D0=0 Right, Down D1:D0=1 Left, Down D1:D0=2 Right, Up D1:D0=3 Left, Up VH=0 Horizontal Direction VH=1 Vertical Direction	00h

▪ D3=0 : Memory Data [D7=Pixel1, D6=Pixel2, D5=Pixel3, D4=Pixel4, D3=Pixel5, D2=Pixel6, D1=Pixel7, D0=Pixel8]

▪ D3=1 : Memory Data [D7=Pixel8, D6=Pixel7, D5=Pixel6, D4=Pixel5, D3=Pixel4, D2=Pixel3, D1=Pixel2, D0=Pixel1]



▪ D3=0

Memory

MSB LSB

7	6	5	4	3	2	1	0
1	1	0	0	1	0	1	0

1 Address = 8 Pixels

⇨ (Default)

Display

COUT0 COUT7

1	1	0	0	1	0	1	0

WriteDirection = 00h,
XDispStart = 00h,
YDispStart = 00h

▪ D3=1

Memory

MSB LSB

7	6	5	4	3	2	1	0
1	1	0	0	1	0	1	0

1 Address = 8 Pixels

⇨

Display

COUT0 COUT7

0	1	0	1	0	0	1	1

WriteDirection = 08h,
XDispStart = 00h,
YDispStart = 00h

1.6. Display Direction

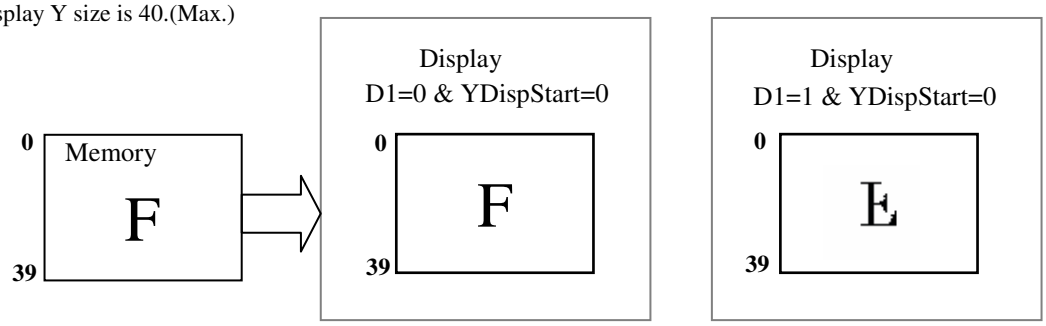
INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	
DispDirection	W	L	**09h**	W	H	-	-	-	-	-	-	D1	D0	-	00h

- Display Direction Set command.
- This command change scan direction of Row.

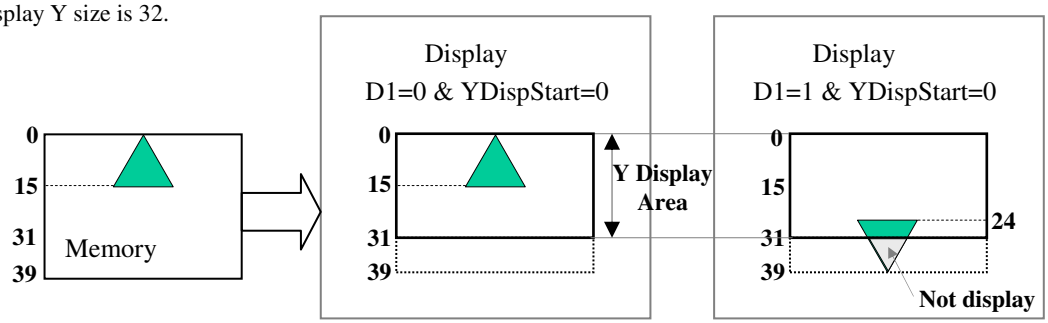
D1	D0	Column	Low
0	0	Min X ⇒ Max X	Min Y ⇒ Max Y
1	0	Min X ⇒ Max X	Max Y ⇒ Min Y

- In "D1=1", display all memory area regardless display size.

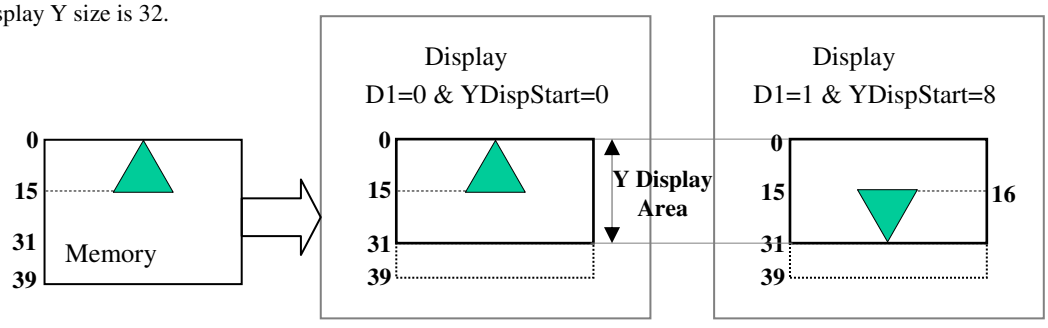
- Display Y size is 40.(Max.)



- Display Y size is 32.



- Display Y size is 32.



1.7. Display Size

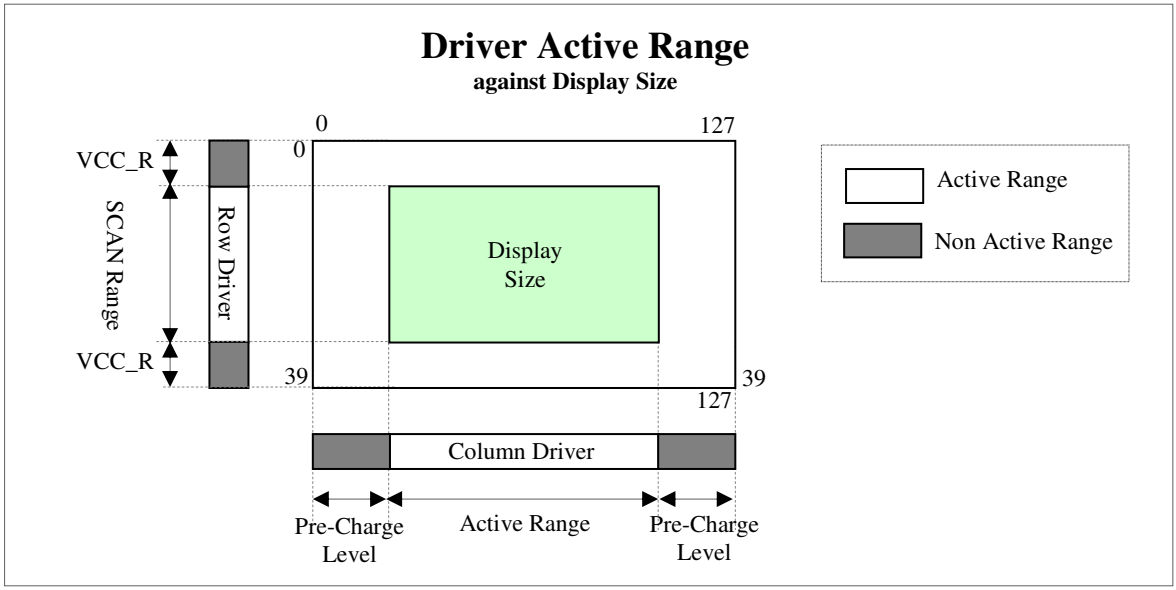
INSTRUCTION	Command			Parameter										Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
DispSizeX	W	L	**30h**	W	H	-	XS6	XS5	XS4	XS3	XS2	XS1	XS0	Column Start Output	00h
				W	H	-	XE6	XE5	XE4	XE3	XE2	XE1	XE0	Column End Output	7Fh
DispSizeY	W	L	**32h**	W	H	-	-	YS5	YS4	YS3	YS2	YS1	YS0	Row Start Output	00h
				W	H	-	-	YE5	YE4	YE3	YE2	YE1	YE0	Row End Output	27h

- Setting Row and Column Outputs Range.

XS6-XS0 : The Start of Column Outputs (Range : 00h-7Fh) (Default 00h)
Setting Value = Pixel number –1
XE6-XE0 : The End of Column Outputs (Range : 00h-7Fh) (Default 7Fh)
Setting Value = Pixel number –1
"XE < XS" is inhibited.

YS5-YS0 : The Start of Row Outputs (Range : 00h-27h) (Default 00h)
Setting Value = Pixel number –1
YE5-YE0 : The End of Row Outputs (Range : 00h-27h) (Default 27h)
Setting Value = Pixel number –1
"YE < YS" is inhibited

*** Notice1: The outputs out of setting range, set Pre-charge level(Column) and VCC_R (Row).**
*** Notice2: Screen Saver Area is moved in all memory Size.**



1.8. Display Start

- This command sets the memory reading start address.

INSTRUCTION	Command			Parameter										Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
XDispStart	W	L	**38h**	W	H	-	DX6	DX5	DX4	DX3	DX2	DX1	DX0	Column Display Start Address	00h
YDispStart	W	L	**39h**	W	H	-	-	DY5	DY4	DY3	DY2	DY1	DY0	Row Display Start Address	00h

- DX6-DX0 : X axis Reading Start address (Range: 00h ~ 7Fh)
- DY5-DY0 : Y axis Reading Start address(Range : 00h ~ 27h)

2. Read / Write command

2.1. Data Reading/Writing Box

INSTRUCTION	Command			Parameter										Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
XBoxAdrrSTART	W	L	**34h**	W	H	-	-	-	-	XS3	XS2	XS1	XS0	Read/Write Box Column Start Address	00h
XBoxAdrrEND	W	L	**35h**	W	H	-	-	-	-	XE3	XE2	XE1	XE0	Read/Write Box Column End Address	0Fh
YBoxAdrrSTART	W	L	**36h**	W	H	-	-	YS5	YS4	YS3	YS2	YS1	YS0	Read/Write Box Row Start Address	00h
YBoxAdrrEnd	W	L	**37h**	W	H	-	-	YE5	YE4	YE3	YE2	YE1	YE0	Read/Write Box Row End Address	27h

- XS3-XS0 : X axis Reading/Writing Start Point (Range: 00h ~ 0Fh)
- XE3-XE0 : X axis Reading/Writing End Point (Range : 00h ~ 0Fh)

- "XE < XS" is inhibited.

- YS5-YS0 : Y axis Reading/Writing Start Point (Range: 00h ~ 27h)
- YE5-YE0 : Y axis Reading/Writing End Point (Range : 00h ~ 27h)

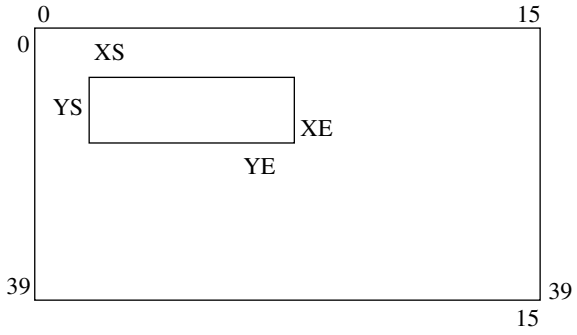
- "YE < YS" is inhibited.

- **After this command executes, writing address is set like under table.**

Writing Direction Mode	X address	Y address
00	**XS**	**YS**
01	**XE**	**YS**
10	**XS**	**YE**
11	**XE**	**YE**

***NOTE : See Writing Direction Set Command.**

Data Writing BOX



2.2. Dot matrix Display Data Read / Write

INSTRUCTION	Command			Parameter										Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
DataRW(Write)	W	L	**08h**	W	H	D7	D6	D5	D4	D3	D2	D1	D0	1 Parameter	-
				:	:	:	:	:	:	:	:	:	:	:	-
				W	H	D7	D6	D5	D4	D3	D2	D1	D0	n Parameter	-
DataRW(Read)	W	L	**08h**	R	H	D7	D6	D5	D4	D3	D2	D1	D0	1 Parameter	-
				:	:	:	:	:	:	:	:	:	:	:	-
				R	H	D7	D6	D5	D4	D3	D2	D1	D0	n Parameter	-

- In the area out of reading / writing-box , this command can't write data.
- Address auto increment acceding to WriteDirection setting direction.
- When memory address increment/decrement is reached at the end of reading / writing-box memory write finish.
- If you read/write again, re-inter "DataRW"command and address is **returned start point**.

Data Write Sequence

Seq	**RW**	**A0**	**DATA BUS**
1.	W	L	RataRW(08h)
2.	W	H	Write 1st Parameter
3.	W	H	Write 2nd Parameter
:	W	H	:
N+1	W	H	Write nth Parameter

Data Read Sequence

Seq	**RW**	**A0**	**DATA BUS**
1.	W	L	RataRW(08h)
2.	R	H	Dummy Read
3.	R	H	Read 1st Parameter
4.	R	H	Read 2nd Parameter
:	R	H	:
N+2	R	H	Read nth Parameter

2.3. **Register Read**

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
READREG	W	L	**20h**	R	H	D7	D6	D5	D4	D3	D2	D1	D0	1st parameter	
				:	:	:	:	:	:	:	:	:	:	:	-
				R	H	D7	D6	D5	D4	D3	D2	D1	D0	Nst parameter	-

Read out all register

Order	**Register**
1	DDISP_ON/OFF
2	DSTBY_ON/OFF
3	DispSize XS
4	DispSize XE
5	DispSize YS
6	DispSize YE
7	ScanMode
8	SleepStart
9	S_Start/Stop

3. Driver Setting command

3.1. Peak Pulse Width Set

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
PaekWidth	W	L	**10h**	W	H	-	-	-	D4	D3	D2	D1	D0	Peak Pulse Width Set D=Width (0-31 SCLK)	05h

Parameter Definition (DCLK Unit)

D[4:0]	**Peak Pulse Width (Default 5SCLK) *1)**
0	0 SCLK
1	1 SCLK
:	:
1Eh	30 SCLK
1Fh	31 SCLK

*1) If conditions is
[(0 < Display Y Size ≤ 16) & (DFRAME(FO) = 1)]
SCLK Frequency : 0.5MHz
else
SCLK Frequency : 1.0MHz.

Refer to “Dot Matrix Frame Rate(**DFRAME**)”

3.2. Peak Pulse Delay Set

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	
PeakDelay	W	L	**16h**	W	H	-	-	-	-	D3	D2	D1	D0	D=Delay(0-7SCLK)	00h

- Parameter Definition (DCLK Unit)

D[3:0]	**Peak Pulse Delay (Default 0SCLK) *1)**
0h	0 SCLK
1h	1 SCLK
:	:
Eh	14 SCLK
Fh	15 SCLK

*1) If conditions is
[(0 < Display Y Size ≤ 16) & (DFRAME(FO) = 1)]
SCLK Frequency : 0.5MHz
else
SCLK Frequency : 1.0MHz.

Refer to “Dot Matrix Frame Rate(DFRAME)”

3.3. Dot Matrix Current Level Set

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	
DotCurrent	W	L	**12h**	W	H	I7	I6	I5	I4	I3	I2	I1	I0	0 – 255μA, 1uA step	00h

- Parameter Definition (1 uA Step)

I[7:0]	**Output Current (Default 0uA)**
00h	0 uA
01h	1 uA
:	:
FEh	254 uA
FFh	255 uA

3.4. Pre-Charge Width Set

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	
PreC_Width	W	L	**18h**	W	H	-	-	-	T4	T3	T2	T1	T0	D=0 : 0-31DCLK	08h

- Parameter Definition (DCLK Unit)

T[4:0]	**Pre-Charge Pulse Width (Default 8 SCLK) *1)**
0h	0 SCLK
1h	1 SCLK
:	:
1Eh	30 SCLK
1Fh	31 SCLK

*1) If conditions is
[(0 < Display Y Size ≤ 16) & (DFRAME(FO) = 1)]
SCLK Frequency : 0.5MHz
else
SCLK Frequency : 1.0MHz.

Refer to “Dot Matrix Frame Rate(DFRAME)”

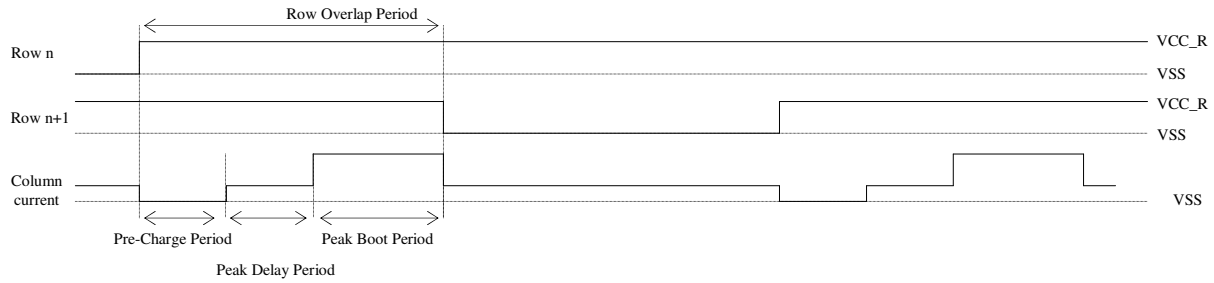
3.5. Pre-Charge Mode Select

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	
PreC_Select	W	L	**44h**	W	H	-	-	-	-	-	-	D1	D0	-	02h

- D1 and D0 used for Pre-Charge and Peak boot Selection Mode.

D1	D0	Pre-Charge	Peak Boot
1	0	Every Time (Default)	Every Time (Default)

3.6. Row Overlap Set



INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
Row_Overlap	W	L	**48h**	W	H	-	-	-	-	-	-	R01	R00	Row overlap Timing	0h

- Row VCC_R timing setting Table.

RO1	**RO0**	**All Row VCC_R Time**
0	0	None (Default)
0	1	Pre-Charge Timing
1	0	Pre-Charge + Peak Delay Timing
1	1	Pre-Charge + Peak Delay + Peak boot Timing

3.7. Row SCAN

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
RowScan	W	L	**17h**	W	H	-	-	-	-	-	-	-	D0	0:Row Scan 1: VSS	00h

- Parameter Definition
  D=”0” normal Scan.
  D=”1” All Row are in VSS.

3.8. Row Scan Sequence Setting

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
ScanMode	W	L	**13h**	W	H	-	-	-	-	-	-	D1	D0	Row Scan Mode	0h

D[1:0]	**SCAN Mode**
0	SCAN Mode
1	Mode 2 : sequential scan mode.
2	Mode 3 : simultaneous scan mode.(half period)

D[1:0]	**DispDirection**	
0	0	R0,R1,R2,…. ,R37,R38,R39,R0,R1,R2, ….
	2	R39,R38,R37,…,R2,R1,R0,R39,R38,R37, ….
1	0	R0,R2…,R36,R38,R1,R3,…R37,R39,R0…
	2	R39,R37…,R3,R1,R38,R36,…R2,R0,R39…
2	0	R0,R2…R38,R0,R2… R1,R3…R39,R1,R3...
	2	R39,R37…R1,R39,R37… R38,R36…R0,R38,R36…

NOTE: DispDirection is 1.6
- In Mode 3, maximum Row number is 20 line at Display Size setting.
  Conditions : [{ 0 ≤ DispSizeY(YS) < 20} and {0 ≤ DispSizeY(YE) < 20}] **or**
  [{ 20 ≤ DispSizeY(YS) < 40}] and {20 ≤ DispSizeY(YE) < 40}]

3.9. Data Reverse

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
Data_Reverse	W	L	**1Ch**	W	H	-	-	-	-	-	RV	D1	D0	Data Reverse	0h

D=0h
When RV =”1” : (Data **EXOR** “FFh”)
When RV =”0” : Memory Data ⇒ Output Data
D=1h : All Output Data are “L”.
D=2h : All Output Data are “H”.

4. Others

4.1. IC Test

This command is only used IC test. Don’t use this command

INSTRUCTION	Command			Parameter									Parameter Definition	Default
	WR	A0	D[7:0]	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
TESTCNT1	W	L	**F0h-FFh**	W	H	D7	D6	D5	D4	D3	D2	D1	D0	1st parameter	
				:	:	:	:	:	:	:	:	:	:	:	-
				W	H	D7	D6	D5	D4	D3	D2	D1	D0	Nst parameter	-

5. Optional Command

5.1. IC Test Command

◇ This command is only used IC test. Don't use this command.

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
TESTCNT0	W	L	**3**				**E**				

5.2. Set Internal Regulator for Row Scan (0x3Fh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
VCC_R_SEL	W	L			**3**		**F**				
Parameter	W	H				**EN**				**D0**	**00h**

"EN" = "1" => Internal regulator enable

"EN" = "0" => Internal regulator disable

* VCC_R pin must be connected to the external voltage source or VCC_C.

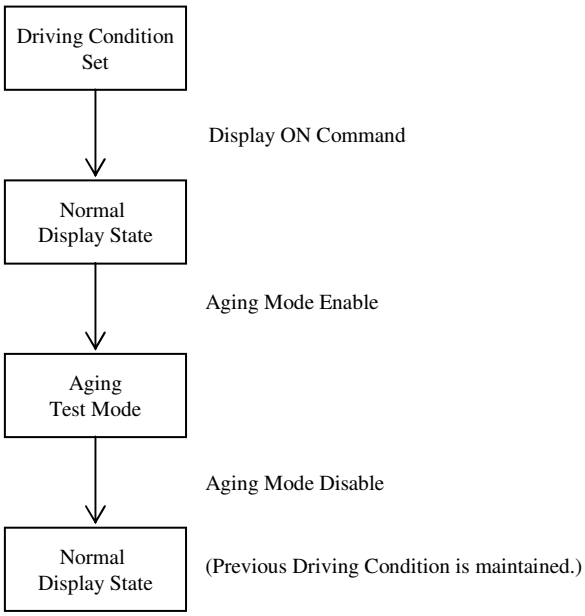
D[0]	VCC_R
0	VCC_C ×0.8
1	VCC_C ×0.7

5.3. AGING Mode Set (3Ch)

INSTRUCTION	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
AGING-EN	W	L	3				C				
Parameer	W	H	-	-	-	-	-	-	-	P0	00h

- If P0 = 0, then AGING Mode is disable.
- If P0 = 1, then AGING Mode is enable.

- This command is used only for aging test mode.
- If P0 = 1, then column state is always forced to the data drive period regardless of the driving conditions.



5.4. Set XTALK Enable (0x3Ah)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
XTALK_EN	W	L			**3**		**A**				
Parameter	W	H								**EN**	**00h**

- If EN = 0, then X-talk function is disable.
- If EN = 1, then X-talk function is enable.

5.5. Dot X-talk Ref. Setting (0x3Bh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
XTALK_Ref	W	L			**3**		**B**				
Parameter0	W	H	-	D6	D5	D4	D3	D2	D1	D0	**00h**
Parameter1	W	H	-	D6	D5	D4	D3	D2	D1	D0	**00h**
Parameter2	W	H	-	D6	D5	D4	D3	D2	D1	D0	**00h**
Parameter29	W	H	-	D6	D5	D4	D3	D2	D1	D0	**00h**
Parameter30	W	H	-	D6	D5	D4	D3	D2	D1	D0	**00h**
Parameter31	W	H	-	D6	D5	D4	D3	D2	D1	D0	**00h**

5.5. Set VDD Selection (0x3Dh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
VDD_SEL	W	L			**3**		**D**				
Parameter	W	H								**D0**	**00h**

- If VDD = 2.8V, D0 = 0
- If VDD = 1.8V, D0 = 1

6. Screen Saver Command

6.1. S_SleepTimer

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_SleepTimer	W	L	**C**				**0**				
Parameter	W	H	**T7**	**T6**	**T5**	**T4**	**T3**	**T2**	**T1**	**T0**	**00h**

◇ S_StepTimer setting Time period 0-255sec. *1)

***1)** Conditions : [1.4. Dot Matrix Frame Rate. FO="1"] and [Display_Y_Size ≤ 16]
S_StepTimer setting Time period 0-510sec. (Step Unit : 2sec)

6.2. S_SleepStart

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_SleepStart	W	L	**C**				**2**				
Parameter	W	H	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**P0**	**00h**

◇ This command stop screen saver and display off after setting time will gone.
P0 = "0" : Sleep Stop.(Default)
P0 = "1" : Sleep Start.
◇ S_SleepStart is execute the follows after setting time will gone.
S_SaverStop (SS = 0h)
S_SleepStart (P0 = 0h)
DDIPS_OFF (P0 = 0h)

6.3. S_StepTimer

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_StepTimer	W	L	**C**				**3**				
Parameter	W	H	**T7**	**T6**	**T5**	**T4**	**T3**	**T2**	**T1**	**T0**	**00h**

◇ Screen Saver event timer setting
T[7:0] : 0~255

6.4. S_StepUnit

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_StepUnit	W	L	**C**				**4**				
Parameter	W	H	**-**	**-**	**-**	**-**	**-**	**-**	**S1**	**S0**	**00h**

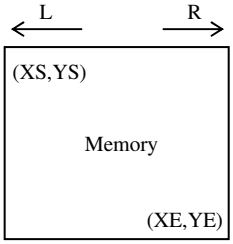
◇ Parameter Definition
Conditions : [1.4. Dot Matrix Frame Rate. FO="0"] or [Display_Y_Size > 16]
S=0 : Timer Stop (Default)
S=1 : 1ms Unit
S=2 : 0.1s Unit

◇ Parameter Definition
Conditions : [1.4. Dot Matrix Frame Rate. FO="1"] and [Display_Y_Size ≤ 16]
S=0 : Timer Stop (Default)
S=1 : 2ms Unit
S=2 : 0.2s Unit

6.5. S_Condition

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_Condition	W	L	**C**				**C**				
Parameter	W	H	-	-	-	-	-	-	**R**	**L**	**00h**

◇ RL : Direction (Default = 0h)



6.6. S_Saver Start/Stop

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_Start/Stop	W	L	**C**				**D**				
Parameter	W	H	-	-	-	-	-	-	-	**SS**	**00h**

SS="0": Screen Saver Stop (Default)
SS="1": Screen Saver Start

6.7. Screen Saver Mode

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_Select	W	L	**C**				**E**				
Parameter	W	H	-	-	-	-	**S3**	**S2**	**S1**	**S0**	**02h**

S[3:0]	Screen Saver Mode
0	-
1	-
2	S_MultiScroll
3	-
4	-
5	-
6	-
7	-
8	-

6.8. S_MultiScroll

◇ Up Down Right Left Scroll.

Time Step	Move Step	Box	LO
Moving by One pixel	1 pixel fixed	No relation	No relation

R	L	Meaning
1	0	Right Scroll
0	1	Left Scroll

I/O INTERFACE PIN MAP (TBD)

PAD #	NAME
1	VSS
2	VCC_R
3	VCC_C
4	IREF
5	VDD
6	VSS
7	RSTB
8	WRB
9	RDB
10	CSB
11	A0
12	D<7>
13	D<6>
14	D<5>
15	D<4>
16	D<3>
17	D<2>
18	D<1>
19	D<0>
20	PS
21	C80
22	EXT_CLK
23	IXS
24	ID2
25	ID1
26	ID0
27	F_SYNC
28	PRE
29	VCC_C
30	VSS

* Command Register

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
01h	SOFTRES	-	-	-	-	-	-	-	-	-
02h	DDISPON/OFF	-	-	-	-	-	-	-	D0	00h
08h	DataRW	D7	D6	D5	D4	D3	D2	D1	D0	-
09h	DispDirection	-	-	-	-	-	-	D1	D0	00h
0Dh	IFMODE	-	-	-	-	-	-	D1	D0	00h
10h	PeakWidth	-	-	-	D4	D3	D2	D1	D0	05h
12h	DotCurrent	D7	D6	D5	D4	D3	D2	D1	D0	00h
13h	ScanMode	-	-	-	-	-	-	D1	D0	00h
14h	DSTBYON/OFF	-	-	-	-	-	-	-	D0	01h
16h	PeakDelay	-	-	-	-	-	D2	D1	D0	00h
17h	RowScan	-	-	-	-	-	-	-	D0	00h
18h	PreCWidth	-	-	-	D4	D3	D2	D1	D0	08h
1Ah	DFRAME	-	-	F0	M1	M0	F2	F1	F0	02h
1Ch	DataReverse	-	-	-	-	-	RV	D1	D0	00h
1Dh	WriteDirection	-	-	-	-	D3	VH	D1	D0	00h
20h	READREG	D7	D6	D5	D4	D3	D2	D1	D0	-
30h	DispSizeX	-	XS6	XS5	XS4	XS3	XS2	XS1	XS0	00h
		-	XE6	XE5	XE4	XE3	XE2	XE1	XE0	7Fh
32h	DispSizeY	-	-	YS5	YS4	YS3	YS2	YS1	YS0	00h
		-	-	YE5	YE4	YE3	YE2	YE1	YE0	27h
34h	XBoxAdrS	-	-	-	-	XS3	XS2	XS1	XS0	00h
35h	XBoxAdrE	-	-	-	-	XE3	XE2	XE1	XE0	0Fh
36h	YBoxAdrS	-	-	YS5	YS4	YS3	YS2	YS1	YS0	00h
37h	YBoxAdrE	-	-	YE5	YE4	YE3	YE2	YE1	YE0	27h
38h	XDispStart	-	DX6	DX5	DX4	DX3	DX2	DX1	DX0	00h
39h	YDispStart	-	-	DY5	DY4	DY3	DY2	DY1	DY0	00h
3Ah	XTALK_EN	-	-	-	-	-	-	-	EN	00h
3Bh	XTALK_REF	-	D6	D5	D4	D3	D2	D1	D0	00h
3Ch	AGING_EN	-	-	-	-	-	-	-	P0	00h
3Dh	VDD_SEL	-	-	-	-	-	-	-	D0	00h
3Fh	VCC_R_SEL	-	-	-	EN	-	-	-	D0	00h
44h	PreC_Select	-	-	-	-	-	-	D1	D0	02h
48h	RowOverlap	-	-	-	-	-	-	RO1	RO0	00h
F0h~FFh	TESTCNT1	D7	D6	D5	D4	D3	D2	D1	D0	-

* Command Register

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
C0h	S_SleepTimer	T7	T6	T5	T4	T3	T2	T1	T0	00h
C2h	S_SleepStart	-	-	-	-	-	-	-	P0	00h
C3h	S_StepTimer	T7	T6	T5	T4	T3	T2	T1	T0	00h
C4h	S_StepUnit	-	-	-	-	-	-	S1	S0	00h
CCh	S_Condition	-	-	-	-	U	D	R	L	00h
CDh	S_Start/Stop	-	-	-	-	-	-	-	SS	00h
CEh	S_Select	-	-	-	-	S3	S2	S1	S0	00h
3Eh	TESTCNT0	D7	D6	D5	D4	D3	D2	D1	D0	-
F0h~FFh	TESTCNT1	D7	D6	D5	D4	D3	D2	D1	D0	-